

WHAT IS CLAIMED IS:

1. A receiver comprising:

a demodulator for receiving symbol signal frames and producing quadrature demodulated output signals;

5 a mapping look-up unit coupled to said demodulator for receiving said quadrature demodulated output signals and determining a three-bit symbol decode associated with points on a predetermined constellation, wherein said constellation has the property of having a first and second point of differing  
10 amplitude and zero reference phase, a third point having an amplitude equal to an amplitude of said first point and a 180 degree reference phase, a fourth point having an amplitude equal to an amplitude of said second point and a 180 degree reference phase, fifth and sixth points having real magnitudes  
15 substantially equal to said amplitude of said first point and equal imaginary magnitudes of opposite sign, and seventh and eighth points having real magnitudes substantially equal to a negation of said amplitude of said first point and equal imaginary magnitudes of opposite sign, wherein said mapping look-  
20 up unit produces probability values for each bit in said three-bit symbol decode from log-likelihood grouping maps for determining membership within a grouping associating said points with values of each bit of said three-bit symbol decode, whereby magnitudes of said quadrature demodulated output signals  
25 determine whether or not each symbol signal frame has membership

in a first subgroup corresponding to a logical zero or membership  
in a second subgroup corresponding to a logical one for each  
grouping; and

a codec coupled to an output of said mapping lookup unit for  
5 receiving said probability values for each bit and determining  
values of each bit.

2. The receiver of Claim 1, wherein said codec comprises a  
forward error correction block coupled to an output of said  
10 mapping look-up unit for receiving said three-bit symbol decode  
from said mapping look-up unit and providing a corrected data  
stream in response to a sequence of three-bit symbol decodes.

3. The receiver of Claim 2, wherein said forward error correction  
15 block is a turbo product decoder.

4. The receiver of Claim 2, wherein said forward error correction  
block is a low density parity check error correction decoder.

20 5. The receiver of Claim 1, wherein said amplitude of said second  
point is substantially equal to three times said amplitude of  
said first point.

6. The receiver of Claim 5, wherein said first through eighth points of said constellation have complex magnitudes of  $(K/2, 0)$ ;  $(3K/2, 0)$ ,  $(K/2, K)$ ,  $(-K/2, K)$ ,  $(-K/2, 0)$ ,  $(-3K/2, 0)$ ,  $(-K/2, K)$  and  $(K/2, K)$ , respectively for a particular rotation of  
s said constellation, where  $K$  is an arbitrary coefficient for determining an overall amplitude of said constellation.

7. The receiver of Claim 1, wherein said amplitude of said first point is less than three times said amplitude of said second  
10 point and greater than the absolute amplitude of said fifth, sixth, seventh and eighth points.

8. The receiver of Claim 1, wherein a grouping associated with a first bit of said three-bit symbol decode divides said constellation between a first subgroup including said first, second, fifth and seventh points and a second subgroup comprising  
5 all points that are not members of said first subgroup, wherein a grouping associated with a second bit of said three-bit symbol decode divides said constellation between a third subgroup including said first, third, seventh and eighth points and a fourth subgroup comprising all points that are not members of  
10 said third subgroup , and wherein a grouping associated with a third bit of said three-bit symbol decode divides said constellation between a fifth subgroup including said first, third, fifth and sixth points and a sixth subgroup comprising all points that are not members of said fifth subgroup, and wherein  
15 said log-likelihood.

9. The receiver of Claim 1, further comprising:

an oscillator coupled to said demodulator for providing a carrier reference for demodulating said symbol signal frames; and  
20 a carrier phase detector coupled to said demodulator for receiving said quadrature demodulated signals and providing an output for controlling a phase of said oscillator, and wherein said carrier phase detector is selectively responsive to a subset of said symbol signal frames in conformity with a detected  
25 amplitude of said quadrature demodulated signals.

10. The receiver of Claim 9, wherein said subset of said symbol signal frames comprises signals corresponding to said first, second, third and fourth members of said constellation.

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11. The receiver of Claim 10, wherein said carrier phase detector comprises a window comparator for determining whether or not an amplitude of one of said symbol signal frames is outside of a predetermined range, and wherein an output of said phase detector  
10 is enabled only when said amplitude of symbol signal frame is outside of said predetermined range.

12. The receiver of Claim 10, further comprising:

a pair of squaring units coupled to said quadrature  
15 demodulated signals; and

a summing unit for summing outputs of said squaring units and providing an output to an input of said window comparator, whereby said window comparator determines whether a square of said amplitude of said symbol signal frame is outside of said  
20 predetermined range.

13. The receiver of Claim 1, wherein said mapping look-up unit includes at least one log-likelihood grouping maps for at least one of said groupings and includes at least one linear decision  
25 map for at least one other of said groupings.

14. A method for receiving a communications signal bearing three-bit symbol encodes associated with points on a predetermined constellation, wherein said constellation has the property of  
5 having a first and second point of differing amplitude and zero reference phase, a third point having an amplitude equal to an amplitude of said first point and a 180 degree reference phase, a fourth point having an amplitude equal to an amplitude of said second point and a 180 degree reference phase, fifth and sixth  
10 points having real magnitudes substantially equal to said amplitude of said first point and equal imaginary magnitudes of opposite sign, and seventh and eighth points having real magnitudes substantially equal to a negation of said amplitude of said first point and equal imaginary magnitudes of opposite sign,  
15 said method comprising:

demodulating a stream of symbol signal frames and producing quadrature demodulated output signals;

retrieving log-likelihood probability values estimating a likelihood of each symbol signal frame being transmitted as each  
20 point of said constellation, each of said probability values retrieved in conformity with values of said quadrature demodulated output signals and for an associated one of said points; and

determining symbols associated with said signal frames in  
25 conformity with said probability values.

15. The method of Claim 14, wherein said determining determines said symbols in conformity with a forward error correction algorithm.

5 16. The method of Claim 15, wherein said forward error correction algorithm computes turbo product decodes.

17. The method of Claim 15, wherein said forward error correction algorithm computes low density parity check decodes.

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18. The method of Claim 14, further comprising generating a carrier reference signal for performing said demodulating, and wherein said generating generates said carrier reference signal phase-locked with a carrier of said stream of symbol signal  
15 frames in response to a phase of some but not all of said points on said predetermined constellation.

19. The method of Claim 14, wherein said generating generates in response to said first, second, third and fourth points on said  
20 predetermined constellation.

20. A receiver comprising:

a demodulator for receiving symbol signal frames and producing quadrature demodulated output signals;

a mapping look-up unit coupled to said demodulator for  
5 receiving said quadrature demodulated output signals and determining a three-bit symbol decode associated with points on a predetermined constellation, wherein said constellation has eight points having complex magnitudes of  $(K/2, 0)$ ,  $(3K/2, 0)$ ,  $(K/2, K)$ ,  $(-K/2, K)$ ,  $(-K/2, 0)$ ,  $(-3K/2, 0)$ ,  $(-K/2, K)$  and  $(K/2, K)$ ,  
10 respectively for a particular rotation of said constellation, where K is an arbitrary coefficient for determining an overall amplitude of said constellation, wherein said mapping look-up unit produces probability values for each bit in said three-bit symbol decode from log-likelihood grouping maps for determining  
15 membership within a grouping associating said points with values of each bit of said three-bit symbol decode, whereby magnitudes of said quadrature demodulated output signals determine whether or not each symbol signal frame has membership in a first subgroup corresponding to a logical zero or membership in a  
20 second subgroup corresponding to a logical one for each grouping, wherein a grouping associated with a first bit of said three-bit symbol decode divides said constellation between a first subgroup including said first, second, fifth and seventh points and a second subgroup comprising all points that are not members of  
25 said first subgroup, wherein a grouping associated with a second

bit of said three-bit symbol decode divides said constellation between a third subgroup including said first, third, seventh and eighth points and a fourth subgroup comprising all points that are not members of said third subgroup , and wherein a grouping  
5 associated with a third bit of said three-bit symbol decode divides said constellation between a fifth subgroup including said first, third, fifth and sixth points and a sixth subgroup comprising all points that are not members of said fifth subgroup; and

10 a forward error correction block coupled to an output of said mapping look-up unit for receiving said three-bit symbol decode from said mapping look-up unit and providing a corrected data stream in response to a sequence of three-bit symbol decodes.

21. The receiver of Claim 20, further comprising:

an oscillator coupled to said demodulator for providing a carrier reference for demodulating said symbol signal frames; and

a carrier phase detector coupled to said demodulator for  
5 receiving said quadrature demodulated signals and providing an output for controlling a phase of said oscillator, and wherein said carrier phase detector comprises a window comparator for enabling an output of said carrier phase detector selectively only in response to signal frames corresponding to said first,  
10 second, third and fourth points of said constellation in conformity with a detected amplitude of said quadrature demodulated signals.

22. A carrier generation circuit for providing a reference signal for demodulating a received sequence of symbol frames decoded as quadrature demodulated signals, said circuit comprising:

an oscillator having an output for providing said reference  
5 signal and an control input for receiving a phase error signal;

a switching circuit having an output coupled to said control input of said oscillator for selectively applying an input phase error signal in response to a switch control input signal;

a phase error magnitude circuit having inputs coupled to  
10 said quadrature demodulated signals for generating said input phase error signal and an output coupled to said switching circuit; and

an amplitude detector having inputs coupled to said quadrature demodulated signals and an output coupled to said  
15 switch control input signal, whereby a phase of said oscillator is controlled in conformity with a subset of said symbol signal frames in conformity with a detected amplitude of said quadrature demodulated signals.

20 23. The circuit of Claim 22, wherein said amplitude detector comprises a window comparator for determining whether or not an amplitude of one of said symbol signal frames is outside of a predetermined range, and wherein said switching circuit is enabled only when said amplitude of symbol signal frame is  
25 outside of said predetermined range.

24. The circuit of Claim 23, wherein said amplitude detector further comprises:

a pair of squaring units coupled to said quadrature demodulated signals; and

5 a summing unit for summing outputs of said squaring units and providing an output to an input of said window comparator, whereby said window comparator determines whether a square of said amplitude of said symbol signal frame is outside of said predetermined range.

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25. The circuit of Claim 22, wherein said phase error magnitude circuit produces said phase error signal in proportion to a first one of said quadrature demodulated signals multiplied by a sign of a second one of said quadrature demodulated signals.